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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,448	04/15/2004	Stephen Wieland	370020-00025	8327

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EXAMINER	
BENSON, WALTER	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/825,448	WIELAND ET AL.	
	Examiner	Art Unit	
	Walter Benson	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☒ Claim(s) 21-23 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 15 April 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are presented for examination.

Drawings

2. The drawings are objected to because where only a single view is used in an application to illustrate the claimed invention, it must not be numbered and the abbreviation "FIG." Must not appear. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

a. Figure 1, page 3, lines 18, 24, 27, and page 6, lines 2 should read "the Figure".

b. page 4, lines 4 and 22, item 46 is identified as emitter 46. In the Figure, item 46 appears to be the collector.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-16, 18-20, are rejected under 35 U.S.C. 102(b) as being anticipated by King Et al. (US Patent No. 4,291,302 and King hereinafter.

6. As to claims 1 and 19, King discloses a fault monitor for an electrical circuit [col. 1, lines 4-7], the circuit having a load, the fault monitor comprising:

a power supply connected in series with a resistor (14,16, Fig. 1; col. 6, lines 7-17);

a connection for connecting to the circuit with the load in parallel with the resistor (Fig. 9; col. 14, lines 60-64);

a voltage sensor connected in series with the resistor (col. 6, lines 11-15);

switching means for opening and closing the connection between the power supply and the resistor and load; whereby a fault within the load will change an equivalent resistance of the load, thereby changing the voltage sensed by the voltage sensor (col. 14, lines 21-30).

7. As to claim 2, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor comprising:

where the switching means includes a first transistor having an entrance connected to the power supply, and an emitter connected to the resistor (col. 13, lines 36-47).

8. As to claim 3, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor comprising:

where the first transistor is a PNP transistor (col. 13, lines 18-19).

9. As to claim 4, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor comprising:

where the switching means includes a second transistor having an entrance connected to the power supply, and an input connected to a switch, with the input of the first transistor connected to the current path controlled by the second transistor (col. 8, lines 36-47).

10. As to claim 5, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor comprising:

where the switch is a resistive voltage switch (col. 8, lines 23-25).

11. As to claim 6, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor further comprising:

a pair of resistors connected in series with the power supply and second transistor, with the input of the first transistor being connected between the pair of resistors (col. 8, lines 59-65).

12. As to claim 7, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor further comprising:

a second resistor connected in series with the power supply, the first transistor, and the resistor', the connector for connection with the circuit being disposed between the resistor and the second resistor (col. 11, lines 454-57).

13. As to claim 8, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor further comprising:

a diode connected in series with the power supply, transistor, and resistor, the diode being structured to resist current flow from the resistor towards the power supply (col. 12, lines 46-52).

14. As to claim 9, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor further comprising:

a capacitor connected in parallel with the load and resistor, and in series with a ground (col. 12, lines 15-17).

15. As to claim 10, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor further comprising:

a capacitor connected in parallel with the voltage sensor and in series with a ground (col. 12, lines 19-23).

16. As to claim 11, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor further comprising:

a Zener diode connected in parallel with the voltage sensor and in series with a ground, the Zener diode being structured to divert current from the voltage sensor if the voltage exceeds a predetermined maximum for the voltage sensor (col. 15, lines 26-34).

17. As to claim 12, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor comprising:

where the breakdown voltage of the Zener diode is about 5.1 volts (col. 12, lines 23-26).

18. As to claim 13, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor comprising:

where the fault monitor is structured to be added to an existing electrical circuit by adding a single connection to the circuit between the power supply and the load (col. 11, lines 3-6).

19. As to claim 14, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor further comprising:

means for determining whether current is flowing within the load (col. 11, lines 23-26).

20. As to claim 15, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor comprising:

where the means for determining whether current is flowing within the load include a test switching means connected in series with the resistor and in parallel with the current sensor, in sequence after the first transistor (col. 12, lines 46-52).

21. As to claim 16, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor comprising:

where the test switching means includes a test transistor having an entrance connected to the power supply, an input connected to a test switch, and an emitter connected to a ground (col. 12, lines 53-55).

22. As to claim 18, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor further comprising:

a resistor between the power supply and the test transistor (col. 13, lines 18-24).

23. As to claim 20, King discloses a fault monitor for an electrical circuit, the circuit having a load, the fault monitor comprising:

where the step of determining whether a failure is present within the load includes determining a number of elements having faults within the load based on the difference between the resulting voltage and an expected voltage (col. 13, lines 24-29).

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over King in view of Kusko et al. (US Patent No. 5,065,104 and Kusko hereinafter).

Although the system disclosed by King shows substantial features of claimed invention (discussed in the paragraphs above), it fails to disclose:

where the test switch is a pull-down resistor switch.

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by King, as evidenced by Kusko.

Kusko discloses a ground fault detector having:

where the test switch is a pull-down resistor switch (col. 16, lines 44-49).

Given the teaching of Kusko, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying King by employing the well known or conventional features of switch devices, such as disclosed by Kusko, in order to efficiently connect the live terminal of the power supply to the load.

Allowable Subject Matter

26. Claims 21-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record fails to teach in combination as claimed a fault monitor providing a test switching device connected in series with the resistor and in parallel with the current sensor, in sequence after the first transistor. Closing the test switching device, and determining whether voltage is sensed by the voltage sensor, thereby determining whether current is flowing through the load.

Prior Art Made of Record

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure

A. Nishioka (US Patent No. 4,661,717) discloses a method and apparatus for sensing a load condition.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter Benson whose telephone number is (571) 272-2227. The examiner can normally be reached on Mon to Fri 6:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Lefkowitz can be reached on (571) 272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter Benson
Patent Examiner

March 1, 2005